

Notice of References Cited	Application/Control No. 09/918,600	Applicant(s)/Patent Under Reexamination TSENG ET AL.	
	Examiner Akash Saxena	Art Unit 2128	Page 1 of 1

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	B	US-6,188,975	02-2001	Gay, Donald L.	703/22
	C	US-5,870,588	02-1999	Rompaey et al.	703/13
	D	US-5,937,185	08-1999	Weir et al.	703/24
	E	US-3,891,974	06-1975	Coulter et al.	703/23
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NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	IEEE Std 1364-1995; IEEE Standard Hardware Description Language Based on the Verilog Hardware Description Language.□□
	V	"A 145 MHz user-programmable gate array"; do Valle Simoes, E. et al;Rapid System Prototyping, 1995. Proceedings., Sixth IEEE International Workshop on 7-9 June 1995 Page(s):226 - 232
	W	Xilinx XC 3000 Technical Data Sheet: Pg 1-3., 1998, Referencedin 1995 from do Valle Simoes above.
	X	"Prototyping Environment for Control-Oriented HW/SW Systems Using State-Charts, Activity-Charts and FPGA's"; Buchenrieder et al; ACM 1994

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.